First Named Inventor	:	Erozan M. Kurtas et al.	
Appln. No.	:		
Filed	:	Herewith	Group Art Unit:
Title	:	TURBO DECODER ARCHITECTURE WITH MINI-TRELLIS SISO	Examiner:
Docket No.	:	I69.12-0554	

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SENT VIA EXPRESS MAIL NO.:

EV 302261041 US

Sir:

The enclosed PTO Form-1449 lists patents and publications submitted pursuant to 37 C.F.R. 1.97. Copies of the patents or publications are enclosed as necessary.

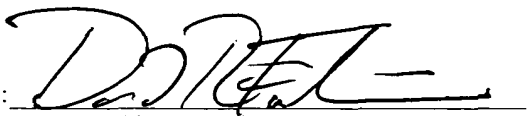
TIME OF FILING

The Information Disclosure Statement is being filed:

1. X with the application or within three months of the filing date of a national application (other than a continued prosecution application under 37 C.F.R. 1.53(d)) or date of entry into the national stage of an international application or, to the best of the undersigned's knowledge, before the mailing date of a first Office action on the merits or a first office action after the filing of a request for continued examination under 37 C.F.R. 1.114, whichever event occurs last. In accordance with 37 C.F.R. 1.97(b), no certification or fee is required.

Respectfully submitted,

KINNEY & LANGE, P.A.

By: 

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FORM PTO-1449	Atty. Docket No.: I69.12-0554	Application No.:
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	First Named Inventor: Erozan M. Kurtas et al.	
	Filing Date: Herewith	Group Art:

U.S. PATENT DOCUMENTS

Examiner Initial		Document No.	Date	Name	Class	Sub Class	Filing Date If Appropriate
	AA	5,812,601	09/22/98	Schramm	375	262	11/15/96
	AB						

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AC	"Reduced Complexity In-Phase/Quadrature-Phase Turbo Equalisation Using Iterative Channel Estimation", B.L. Yeap, et al., *0-7803-7097-1/01 IEEE*, 2001.
	AD	"A Soft-Input Soft-Output Maximum A Posteriori (MAP) Module to Decode Parallel and Serial Concatenated Codes", S. Benedetto, et al., *TDA Progress Report 42-127*, November 15, 1996.
	AE	"Convergence Properties of Iterative Decoders Working at BIT and Symbol Level", B. Scanavino, et al. Politecnico de Torino, Torino, Italy.
	AF	"VLSI Architectures for Turbo Codes", Guido Masera, et al., *IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS*, Vol. 7, No. 3, September 1999.
	AG	"SCTCM with Inner Rate-1 Accumulate Code" (printed slide presentation), Hugo M. Tullberg and Paul H. Siegel, Signal Transmission and Recording Group, UCLA, January 30, 2002.
	AH	"Serial Concatenated Trellis Coded Modulation with Inner Rate-1 Accumulate Code", Hugo M. Tullgerg and Paul H. Siegel, *0-7803-7208-5/01 IEEE*, 2001.
	AI	"On Joint Iterative Decoding of Variable-length Source Codes and Channel Codes", Ahmadreza Hedayat and Aria Nosratinia, Multimedia Communications Laboratory, Richardson, TX.
	AJ	"Trellis Turbo-Codes in Flat Rayleigh Fading with Diversity", Christos Komninakis and Richard D. Wesel, *0-7803-7206-9/01 IEEE*, 2001.
	AK	"A Low Latency SISO with Application to Broadband Turbo Decoding", Peter A. Beerel and Keith M. Chugg, *IEEE JOURNAL ON SELECTED AREAS IN COMMUNICATIONS, Vol. 19, No. 5*, May 2001.
	AL	"Further Results on a Reduced-Complexity, Highly Power-/Bandwidth-Efficient Coded Feher-Patented Quadrature-Phase-Shift-Keying System with Iterative Decoding", M.K. Simon and D. Divsalar, *IPN Progress Report 42-146*, August 15, 2001.
	AM	"A Soft-Input Soft-Output APP Module for Iterative Decoding of Concatenated Codes", S. Benedetto, et al., *IEEE COMMUNICATIONS LETTERS, Vol. 1, No. 1*, January 1997.

EXAMINER: DATE CONSIDERED:

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.